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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.     | CONFIRMATION NO.       |
|--|-------------|----------------------|-------------------------|------------------------|
| 10/524,749   | 02/15/2005  | Hiroyuki Yoshida     | 09792909-6113           | 6915                   |
| 26263 7590 07/11/2007<br>SONNENSCHN NATH & ROSENTHAL LLP<br>P.O. BOX 061080<br>WACKER DRIVE STATION, SEARS TOWER<br>CHICAGO, IL 60606-1080 |             |                      | EXAMINER<br>KALAM, ABUL |                        |
|  |             |                      | ART UNIT<br>2814        | PAPER NUMBER           |
|  |             |                      | MAIL DATE<br>07/11/2007 | DELIVERY MODE<br>PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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**Office Action Summary**

Application No.

10/524,749

Applicant(s)

YOSHIDA, HIROYUKI

Examiner

Abul Kalam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3,6 and 7 is/are pending in the application.
- 4a) Of the above claim(s) 1-3 and 6 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 February 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

***Continued Examination***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 1, 2007 has been entered.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 7** is rejected under 35 U.S.C. 102(b) as being anticipated by **Chung et al.** (US 6,218,691, previously cited).

With respect to **claim 7**, **Chung** teaches a method of manufacturing an image pickup device having at least one insulated gate field effect transistor (**S<sub>x</sub>**, “**select transistor**”) in an output circuit (**col. 3: lns. 52-53**) of the image pickup device and are formed in a substrate (**500**), said method comprising the steps of (**FIGS. 4 and 5A-5D**):

forming, prior to forming said insulated gate field effect transistor, a first diffusion layer (**501, P-EPI; FIG. 5A**) of a first conduction type (**P-type**) in said substrate (**500**) beneath where said insulated gate field effect transistor (**S<sub>x</sub>; FIG. 4**) is to be formed, at a position deeper than a region where a source region and a drain region of said insulated

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gate field effect transistor are to be formed (**N+ diffusion regions located below the gate of select transistor ( $S_x$ ) in the P-WELL, as shown in FIG. 4, are interpreted as the source/drain regions of the select transistor**), the first diffusion layer (**501, P-EPI**) underlying an entire area of said source and an entire area of said drain region (**N+ diffusion regions as describe above**) and entirely separated from said source region and drain region (**P-WELL entirely separates the source/drain regions (N+ diffusion regions) from the first diffusion layer (501)**); and

forming, prior to forming said insulated gate field effect transistor and at a different time than the step of forming the first diffusion layer, a second diffusion layer (**P+SUB 500, FIG. 5D**) of the first conduction type (**P-type**) having a higher concentration (**P+**) than said first diffusion layer (**P-EPI**) in said substrate at a position deeper than said first diffusion layer (**FIG. 5A**), the second diffusion layer (**P-EIP**) being entirely separated from said first diffusion layer (**P+SUB**) by an intervening layer (**N-TYPE BURIED LAYER; FIG. 5C**) having a conduction type (**N-type**) that is different than the first conduction type (**P-type**) (**col. 3: Ins. 20-25, 62-66; col. 4: Ins. 1-20**).

### ***Response to Arguments***

3. Applicant's arguments with respect to claim 7, filed on May 1, 2007 have been considered but are not persuasive.

Applicant argues that Chung does not teach wherein the second diffusion layer is formed at a different time than the step of forming the first diffusion layer. This is not persuasive because **Chung** clearly shows that the second diffusion layer (**P+SUB, 500**;

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**FIG. 5A)** is formed before the step of forming the first diffusion layer (**Part of P-EPI 501 within the N-type buried layer 508a; FIG. 5D)** (col. 3: Ins. 62-66, col. 4: Ins. 1-20).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abul Kalam



PHAT X. CAO  
PRIMARY EXAMINER